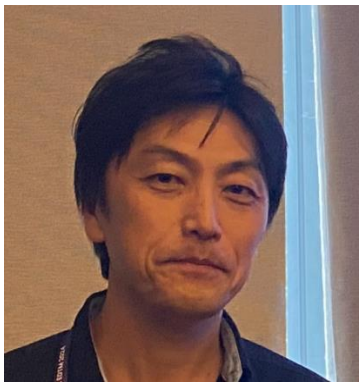
NVMTS 2024

October 21-23, 2024 l Paradise Hotel Busan (Haeundae Beach), Busan, Korea



Tomoya Sanuki

(KIOXIA, Japan)

Tomoya Sanuki received the M.Sc. degree in physics from Osaka University, Japan. In 1999, he joined Toshiba Corporation, where he was engaged in the research and development of advanced CMOS Logic, embedded DRAM and system LSI at Device Technology Laboratory. In 2015, he became a researcher and device engineer at Institute of Memory Technology R&D, where he was involved in the development of magnetic RAM, 3D flash memory and future device technology. Since 2024, he has been a senior researcher and strategist at Frontier Technology R&D Institute in KIOXIA. He has 95+ U.S. patents issued or pending in the area of new semiconductor devices and authored or co-authored 25+ publications in IEDM, VLSI, EDTM, JXCDC and IMW. He also had been served as technical committees at various conferences including EDTM, VLSI-TSA, and IMW.